Wideband Amplifier/Multiplier

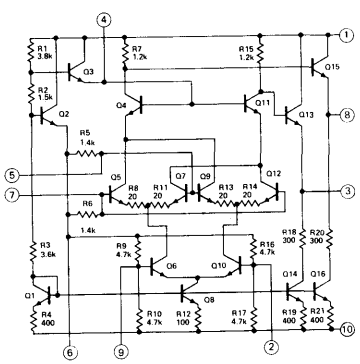
SG1402/2402/3402 are monolithic four quadrant multipliers offering excellent frequency response and provision for use as a variable gain amplifier with both non-inverting and inverting outputs available. In addition to linear amplification, the device is also ideal for balanced modulation, pulse or gated amplification, and coincidence detection.

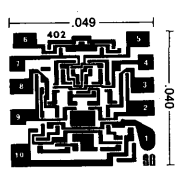
- **Single power supply voltage**
- **Self-contained biasing**
- **25dB voltage gain**
- **Differential or single ended inputs and outputs**
- **Large bandwidth**
- **Low power dissipation**

PARAMETERS, CONDITIONS*	1402	2402	3402	UNITS
Supply Voltage	+18		+18	V
Load Current	15		15	mA
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	°C
Package Types	J, T	J, T, N		–
Maximum Voltage Gain, single ended	23		20	dB
Variable Gain Range, with ext. balance	55		40	dB
Frequency Response, f − 3 dB	40 (min)		50 (typ)	MHz
Input Impedance, Pin 5 or 7 (7 or 10)[1]	1.2 (typ)		1.2 (typ)	KΩ
Input Impedance, Pin 2 or 9 (3 or 12)[1]	1.8 (typ)		1.8	KΩ
Output Impedance, Pin 3 or 8 (4 or 11)[1]	100 (typ)		100 (typ)	Ω
Output Voltage Swing R_L = 100K R_L = 1K	 3 1.3		 3 1.3	Vpp
Quiescent DC Levels Pins 5, 6 and 7 (7, 8 & 10)[1]	3.6 (typ)		3.6 (typ)	V
Pins 2 and 9 (3 & 12)[1]	1.8 (typ)		1.8 (typ)	V
Pins 3 and 8 (4 & 11)[1]	6.5/7.5		7.0 (typ)	V
Output Offset Voltage Minimum Gain Maximum Gain	 100 200		 300 500	mV
DC Output Shift, with max gain change	100		200	mV
Differential Control Voltage, for max gain change	200 (typ)		200 (typ)	mV
Maximum Gain Variation, over temperature	2		3	dB
Equivalent Input Noise (BW = 10MHz, R_S = 50Ω)	25 (typ)		25	μVrms
Power Consumption	85		85	mW

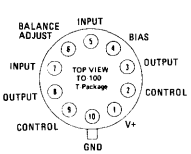
*Parameters are for T_A = 25°C, V^+ = 10V, f = 100KHz and are min./max. limits unless otherwise specified.

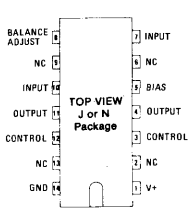
[1]Numbers in parentheses refer to dual-in-line package.



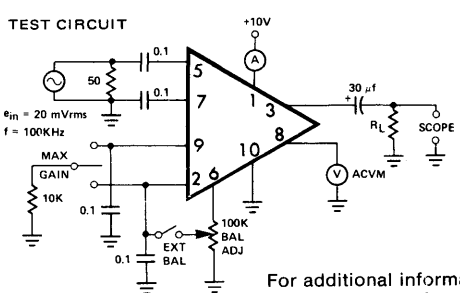


SG1402/2402/3402 Chip (See T-package diagram for pad functions)





CONNECTION DIAGRAMS



See Applications Notes for additional information.

For additional information on this device, refer to Applications Notes.

INTRODUCTION

Rapid advances in the state-of-the-art of processing monolithic linear integrated circuits have made the use of tightly matched components a practical reality. This in turn has opened the doors to a new class of circuit characterized by its utility, versatility, and ease of application. It is now possible to include on a monolithic chip, many of the components which, because of relatively poor tolerances, were formerly required to be external to the circuit. The SG1402, shown schematically in Figure 1, illustrates this capability both by its inclusion of all necessary biasing networks and by the nature of the circuit itself which requires extremely well matched component parameters for successful operation.

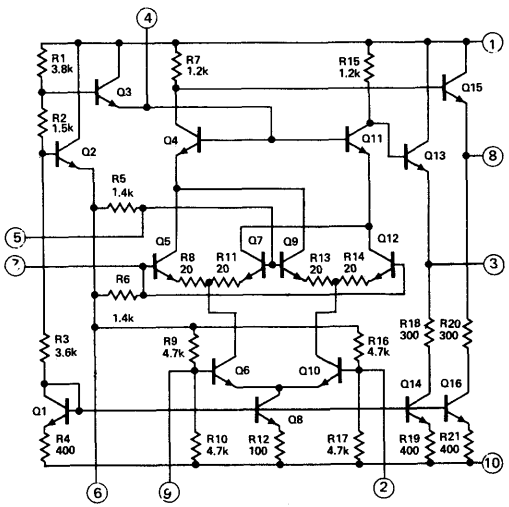


Figure 1. SG1402 Schematic Diagram.

HOW IT WORKS

The heart of the SG1402 is a four quadrant multiplier consisting of two cross-coupled differential amplifiers which are jointly controlled by a third differential amplifier. This part of the circuit is shown in simplified form as Figure 2. The constant current, I_0, is divided by Q6 and Q10 and divided again by each of the upper diff amps such that, for balanced operation, transistors Q5, Q7, Q9, and Q12 each have ¼ I_0 flowing through them. An examination of the way in which the above diff amps are cross-coupled will show that while the collector load resistors receive a portion of their current from each diff amp, the signals will arrive out of phase with respect to each other. This is because the input voltage, v_c, is amplified common emitter – with 180° phase shift – through Q9 and summed at resistor R7 with the signal which has gone common collector-common base – with 0° phase shift – through Q7 and Q5. Therefore, with the circuit perfectly balanced, the two signals completely cancel out and the output has zero signal. This can be shown mathematically as follows:

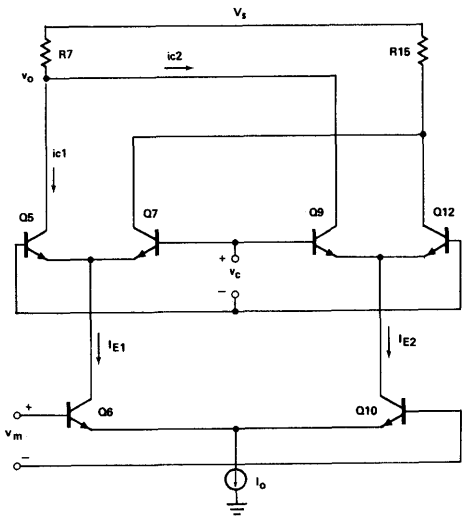


Figure 2. Simplified Schematic of the Multiplier Section of the SG1402.

The collector current in one side of a simple differential amplifier (Q5 and Q7, for example) is:

$$i_{c1} = \frac{I_{E1}}{1 + \exp\left(\frac{q}{kT} v_c\right)}$$

where: I_{E1} = sum of currents in each collector

$\frac{kT}{q}$ = 26 millivolts at 25°C

v_c = differential input voltage

This equation can be differentiated to obtain the transconductance which, for small values of v_c, is:

$$gm = \frac{di_{c1}}{d\,v_c} = \frac{q\,I_{E1}}{4kT}$$

In a similar manner, the transconductance through Q9 is:

$$gm = \frac{di_{c2}}{d\,v_c} = \frac{q\,I_{E2}}{4kT}$$

and the total voltage gain, Av is:

$$Av = R_L \frac{di_{c1}}{d\,v_c} + \frac{di_{c2}}{d\,v_c}$$

$$= \frac{R_L\,q}{4kT}\left(I_{E2} - I_{E1}\right)$$

Since $I_{E1} + I_{E2} = I_0$, it can be seen that when $v_m = 0$, $I_{E1} = I_{E2} = \frac{1}{2} I_0$ and Av = 0. With I_{E1} and I_{E2} being collector currents of another differential amplifier, the total small-signal gain equation may be written:

$$Av = \frac{v_0}{v_c} = \frac{R_L I_0 q}{4\ kT}\left[\frac{1}{1+\exp\left(\frac{q}{kT} v_m\right)} - \frac{1}{1+\exp\left(\frac{q}{-kT} v_m\right)}\right]$$

The circuit gain of the SG1402 is less than that predicted by the above equation due to the local feedback offered by the 20 ohm emitter resistors. The actual relationship between Av and v_m is shown in Figure 3 while Figure 4 graphs the full four-quadrant transfer function between the input voltage, v_c, the control voltage, v_m, and the output voltage. Note that the 20 ohm emitter resistors provide linearity for ±60 millivolts of input voltage while the modulating voltage is only linear for approximately half that value. It should be recognized from Figure 4 that output limiting occurs at a constant input voltage regardless of the modulating voltage. In other words, reducing the gain reduces the maximum peak-to-peak output swing.

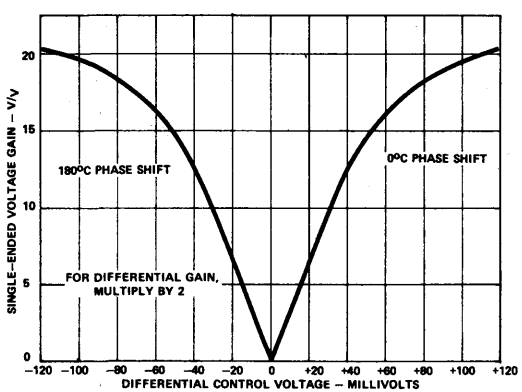


Figure 3. Differential Gain Control.

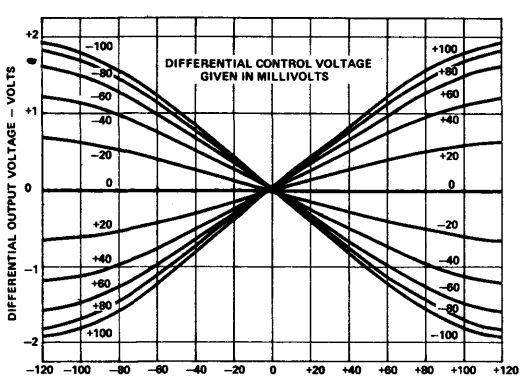


Figure 4. Multiplier Transfer Function.

BIASING CIRCUITRY

Key to the utility of the SG1402 is the inclusion of all the biasing and level shifting circuitry normally required as external components. This is provided by matched current sources and low impedance voltage sources.

Resistors R1, R2, R3 and R4 are directly across the supply voltage and establish a current:

$$I_b = \frac{V_S - V_{BEQ1}}{R1 + R2 + R3 + R4} = 1\ \text{mA at 10 volts}$$

Transistors Q14 and Q16 have the same geometries and emitter resistors as Q1 and therefore, with the same base voltage, they each are also conducting one milliamp and provide the loads for the output emitter followers, Q13 and Q15. This saves chip area as a transistor requires less space than a resistor which would establish the same current.

Transistor Q8 has four times the emitter area and ¼ the emitter resistor as Q1 and thus defines a current level I_0 of 4 milliamps.

The bias voltage levels required at different points in the circuit are all defined by the same resistors which set the current levels but there is no mutual interaction due to the insertion of Q2 and Q3 which act as low-impedance isolators.

Transistors Q4 and Q11 serve only as common-base stages to isolate the load resistor from the collector capacitance of the parallel diff-amp transistors. Thus, frequency response is improved with only slight increase in circuit complexity.

The chip layout of the SG1402 was done to optimize the component matching regardless of mask registration and process variations. From the photomicrograph shown in Figure 5, it can be seen how the symmetrical nature of the circuit was exploited to obtain matched parameters. The chip has an area of 48 by 39 mils.

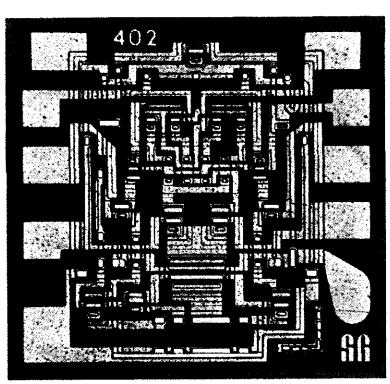


Figure 5. Photomicrograph of SG1402 Chip.

VARIABLE GAIN AMPLIFICATION

The circuit of Figure 6 shows the simplest application of the SG1402 as a single-ended, variable-gain amplifier. The signals at the two outputs are always equal in magnitude and opposite in phase. As the gain control potentiometer is moved from one end to the other, each output will start with a maximum signal, reduce to a minimum when the pot is centered, and increase to maximum again in the opposite phase as the wiper gets to the other end of the potentiometer.

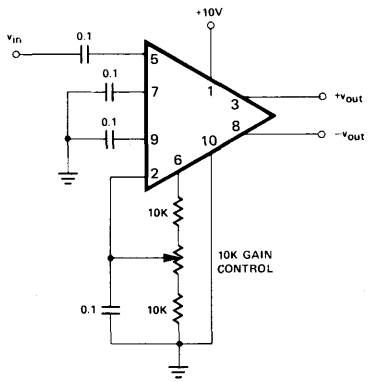


Figure 6. Single-Ended Variable-Gain Amplifier Configuration with Manual Gain Control to Provide Maximum Output of Either Phase.

For applications where a phase change is not desired, the incorporation of a diode as shown in Figure 7 will allow a DC control voltage to vary the input-output transfer function from a gain of +25 dB to an attenuation of −25 dB. This relationship is plotted in the graph of Figure 8.

Since this change in transfer function is accomplished with no net change in either operating currents or bias levels, it is transient-free and extremely fast-reacting. Thus, the circuit of Figure 7 may also be used as a gated amplifier with the control requirements compatible with 0 to 5 volt logic levels. The waveform in Figure 9 shows a 1 MHz signal controlled with a 10 microsecond pulse.

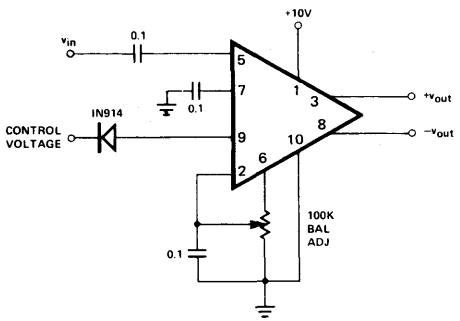


Figure 7. Addition of Diode Provides Gain Control Without Phase Change. Balance May be Eliminated if Maximum Attenuation is not Required.

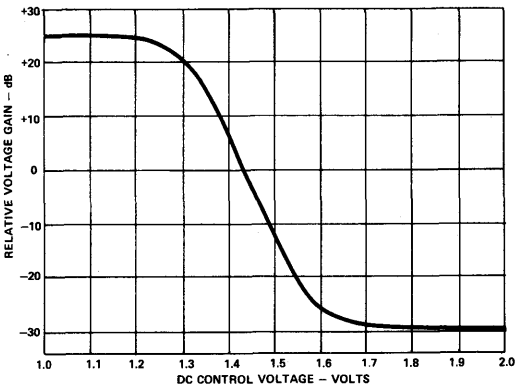


Figure 8. Gain Variation as a Function of Control Voltage with Diode Coupled Input.

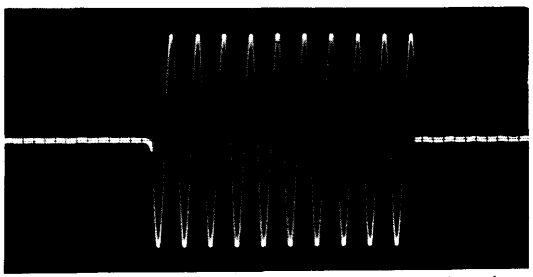


Figure 9. Gate Amplifier or Pulse Modulator Response. Input is 10 mVrms, 1 MHz and Control Voltage is 0 to 5 Volt Square Wave with f = 50 kHz.

MODULATION

The multiplying function of the SG1402 can be used to provide both balanced and amplitude modulation utilizing the basic circuit shown in Figure 10. With the potentiometer adjusted for optimum balance, the carrier signal is canceled out producing a doublesideband waveform at the output. Depending upon the amplitude of the carrier signal, higher frequency harmonics can also be generated; however, if only the lower sideband is used, filtering of the upper sideband will also eliminate all the harmonics. It should be noted that this balanced modulation is achieved without the need for the usual transformers and only capacitive coupling is required. Typical waveforms are shown in Figure 11.

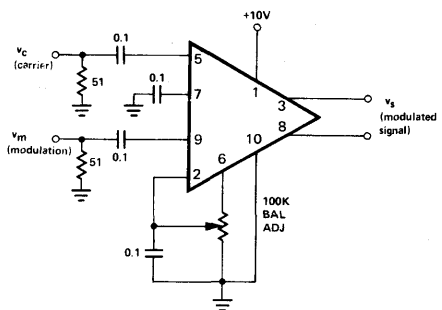


Figure 10. Balanced Modulator.

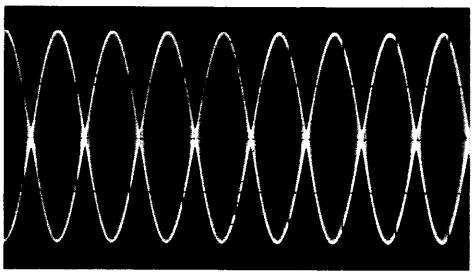


Figure 11. Balanced Modulator Output Waveform. (0.1V/cm, 50 μs/cm, f_c = 1 MHz, f_m = 10 KHz).

If the potentiometer is adjusted so that the circuit is unbalanced, then the carrier is included in the output signal and amplitude modulation as shown in Figure 12 results. The optimum adjustment can most readily be made while observing the output waveform on an oscilloscope. Care should be taken that neither signal overdrive the circuit.

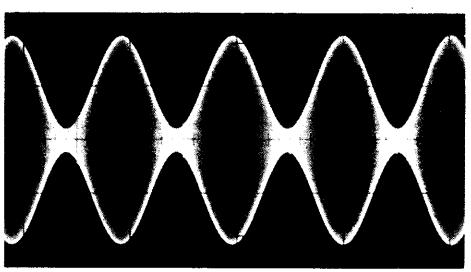


Figure 12. Amplitude Modulator Output Waveform. (0.2V/cm, 50 μs/div, f_c = 1 MHz, f_m = 10 KHz).

By using a signal to modulate itself with the circuit shown in Figure 13, the input is squared and since

$$\cos^2 \omega t = \tfrac{1}{2} [1 + \cos 2 \omega t]$$

the output frequency is twice that of the input. Typical waveforms for this frequency doubler application are shown in Figure 14.

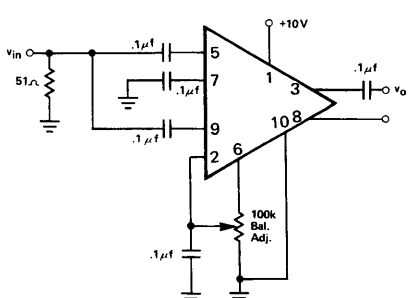


Figure 13. Frequency Doubler.

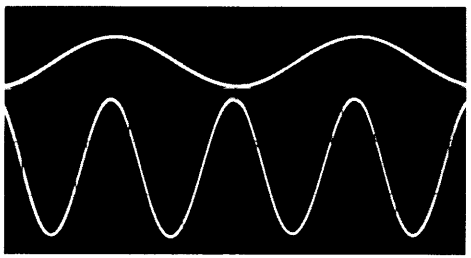


Figure 14. Frequency Doubler Input and Output Waveform. (50mV/cm, 0.2 μs/div, f_1 = 1 MHz, f_2 = 2 MHz).

DEMODULATORS

The same features which make the SG1402 an excellent modulator provide superior performance when the circuit is used as a single or double sideband demodulator. The circuit of Figure 15 illustrates the simplicity of this application. The balance pot is not necessary since the inserted carrier is eliminated by the low-pass filter at the output.

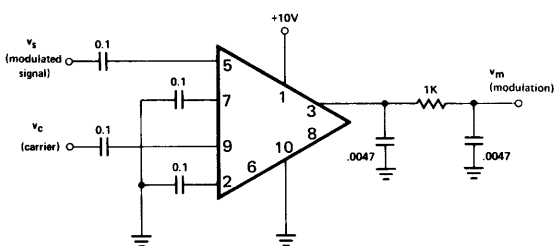


Figure 15. Balanced Demodulator.

The same general approach may be used for amplitude modulation and a block diagram of a simple AM detector is shown in Figure 16. Thus, the SG1402 can be used in receivers which combine SSB and AM to provide complete signal transformation in either mode of operation.

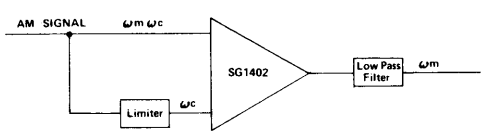


Figure 16. AM Detector Block Diagram.

CONCLUSIONS

With the introduction of the SG1402, Silicon General has provided a powerful tool to the communications engineer and all others working with information processing. Because of its versatility and capability, this device opens the way to a much greater utilization of carrier transmission schemes for data handling in applications ranging from outer space to home kitchens.