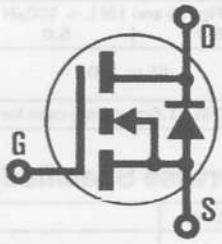
PD-9.327

INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF710 IRF711 IRF712 IRF713



N-Channel

400 Volt, 3.6 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

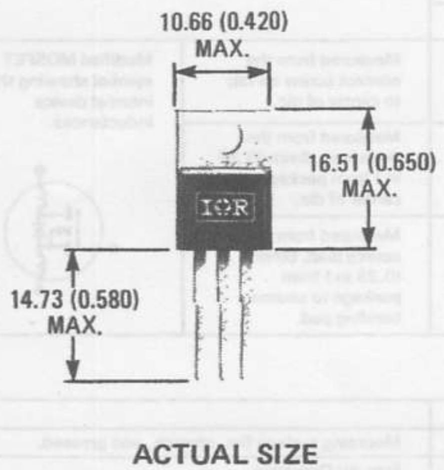
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

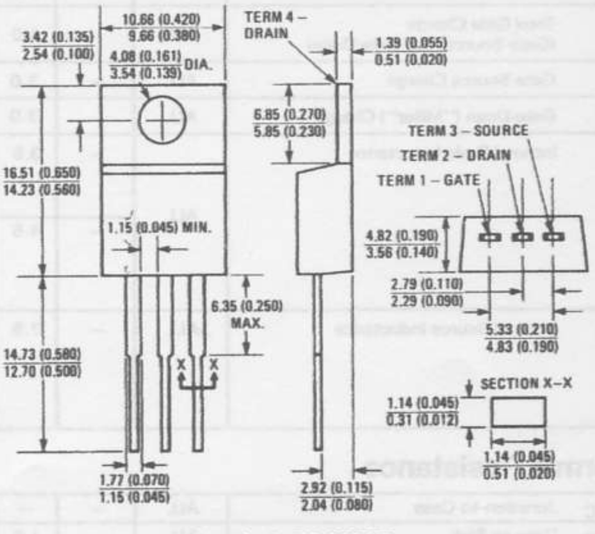
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF710	400V	3.6Ω	1.5A
IRF711	350V	3.6Ω	1.5A
IRF712	400V	5.0Ω	1.3A
IRF713	350V	5.0Ω	1.3A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

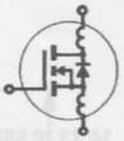
Absolute Maximum Ratings

	Parameter	IRF710	IRF711	IRF712	IRF713	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	1.5	1.5	1.3	1.3	A
I_D @ T_C = 100°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current ③	6.0	6.0	5.0	5.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 6.0	6.0	5.0	5.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF710 IRF712	400	—	—	V	V_{GS} = 0V
		IRF711 IRF713	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF710 IRF711	1.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF712 IRF713	1.3	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF710 IRF711	—	3.3	3.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRF712 IRF713	—	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 0.8A
C_{iss}	Input Capacitance	ALL	—	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	35	50	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	8.0	15	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	3.0	10	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 0.8A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	5.0	10	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	6.0	7.5	nC	V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	3.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF710 IRF711	–	–	1.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF712 IRF713	–	–	1.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF710 IRF711	–	–	6.0	A	
		IRF712 IRF713	–	–	5.0	A	
V_{SD}	Diode Forward Voltage ②	IRF710 IRF711	–	–	1.6	V	$T_C = 25°C, I_S = 1.5A, V_{GS} = 0V$
		IRF712 IRF713	–	–	1.5	V	$T_C = 25°C, I_S = 1.3A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	–	380	–	ns	$T_J = 150°C, I_F = 1.5A, dI_F/dt = 100\ A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	–	2.7	–	μC	$T_J = 150°C, I_F = 1.5A, dI_F/dt = 100\ A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

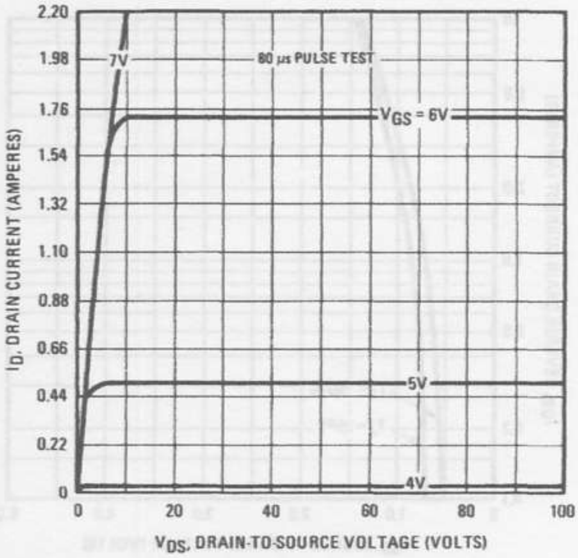


Fig. 1 – Typical Output Characteristics

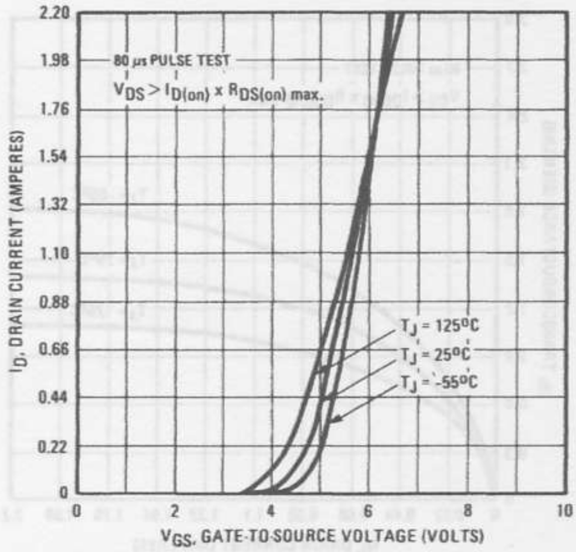


Fig. 2 – Typical Transfer Characteristics

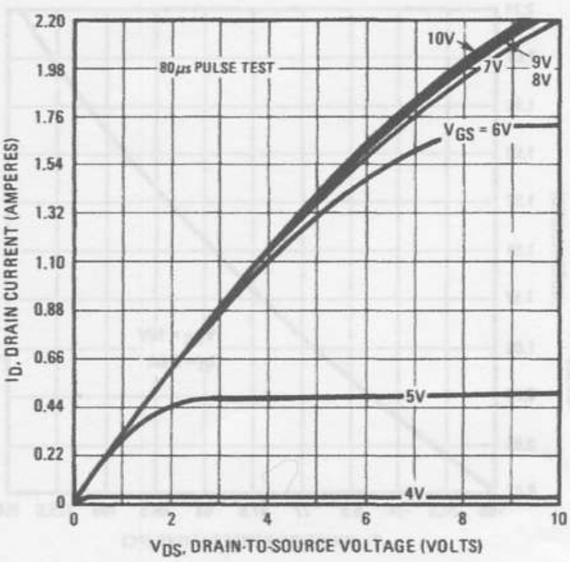


Fig. 3 – Typical Saturation Characteristics

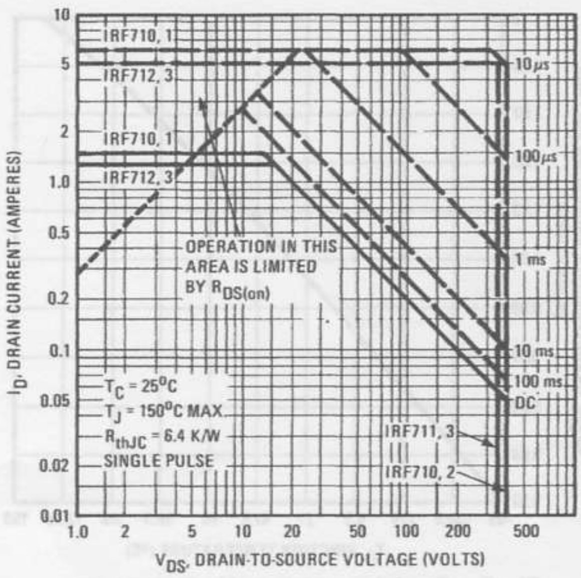


Fig. 4 – Maximum Safe Operating Area

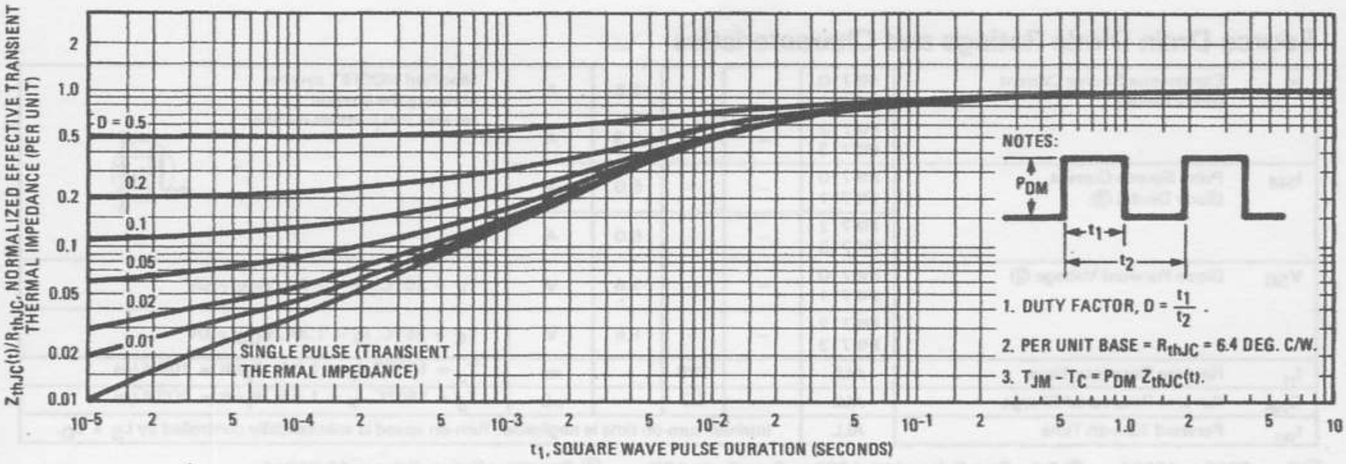


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

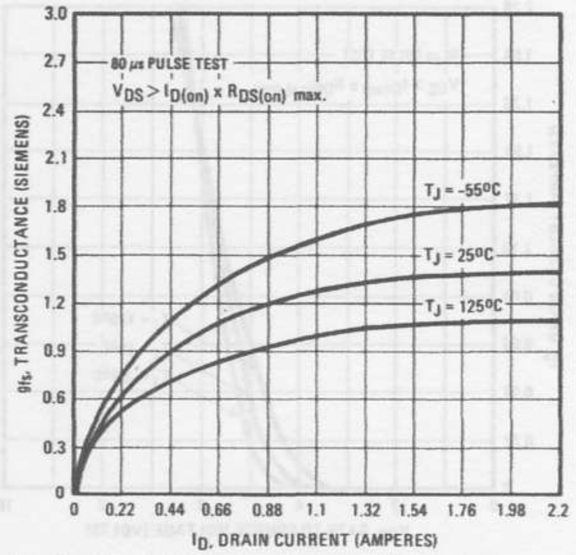


Fig. 6 — Typical Transconductance Vs. Drain Current

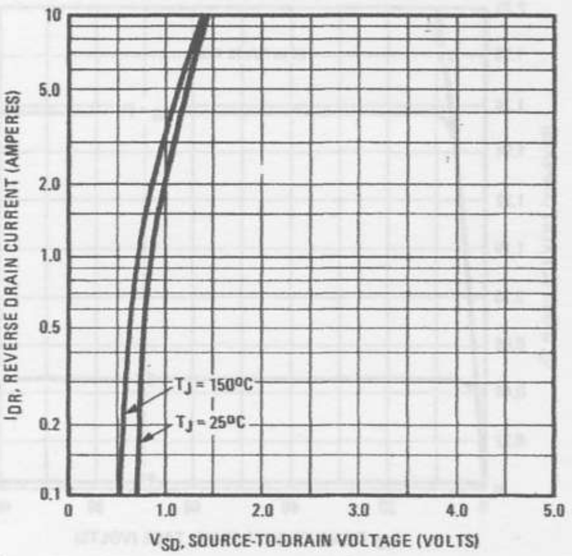


Fig. 7 — Typical Source-Drain Diode Forward Voltage

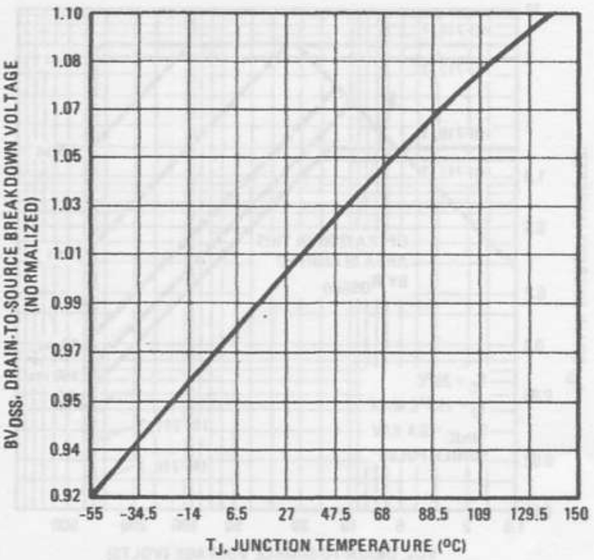


Fig. 8 — Breakdown Voltage Vs. Temperature

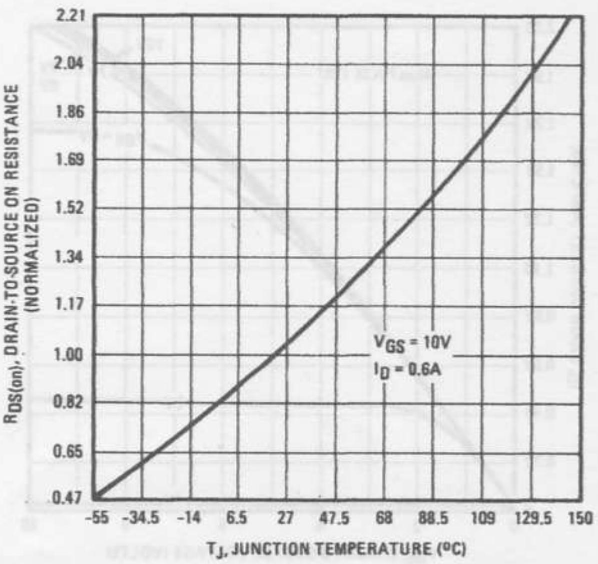


Fig. 9 — Normalized On-Resistance Vs. Temperature

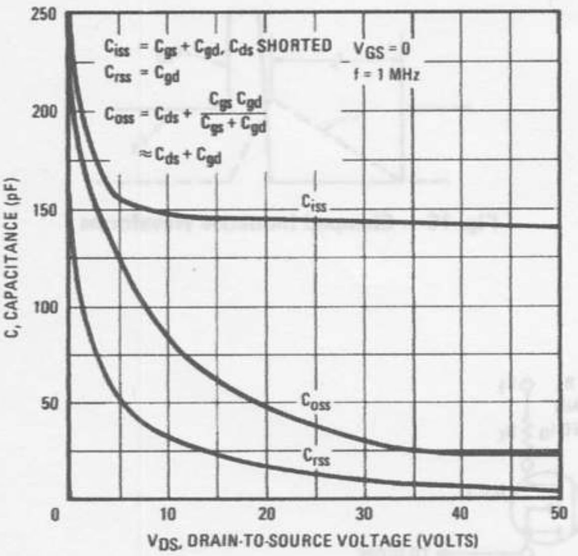


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

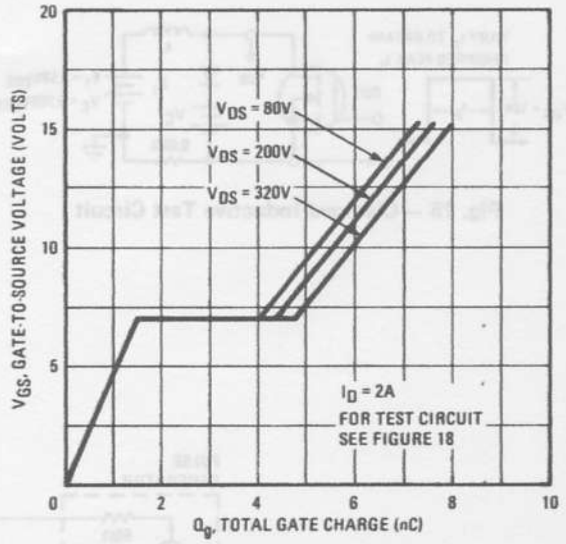


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

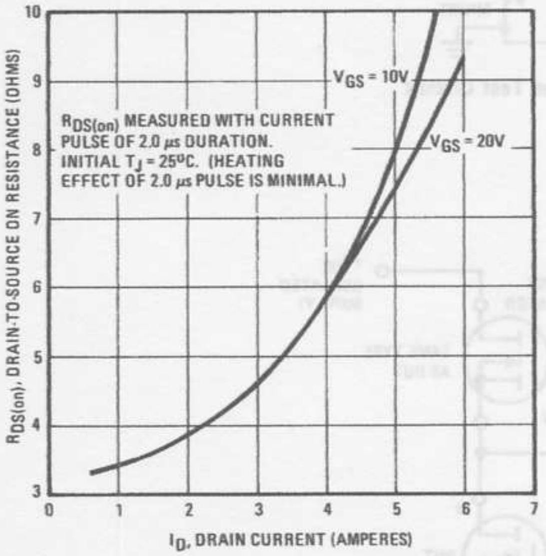


Fig. 12 — Typical On-Resistance Vs. Drain Current

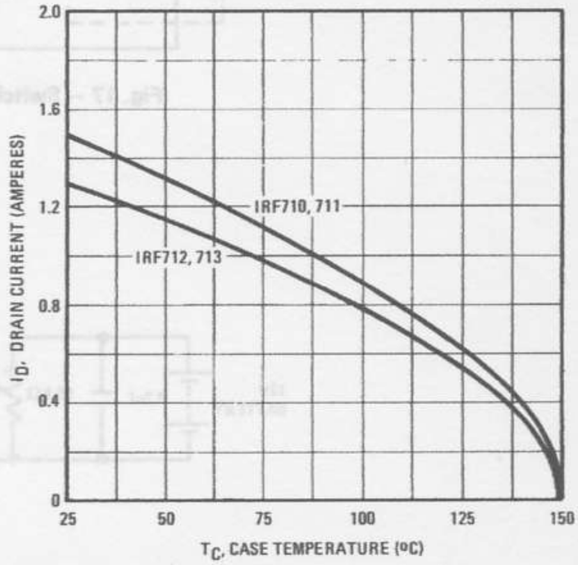


Fig. 13 — Maximum Drain Current Vs. Case Temperature

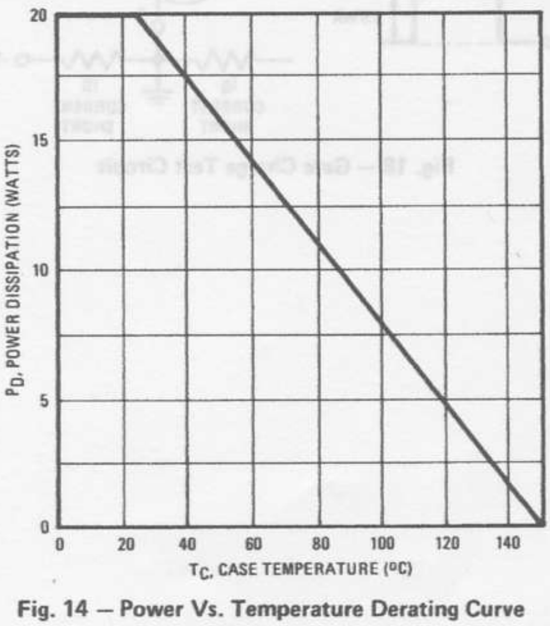


Fig. 14 — Power Vs. Temperature Derating Curve

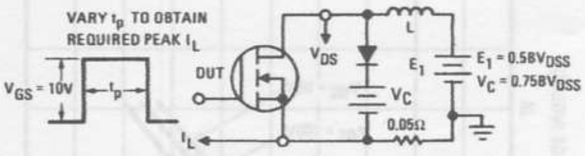


Fig. 15 – Clamped Inductive Test Circuit

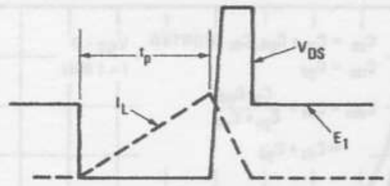


Fig. 16 – Clamped Inductive Waveforms

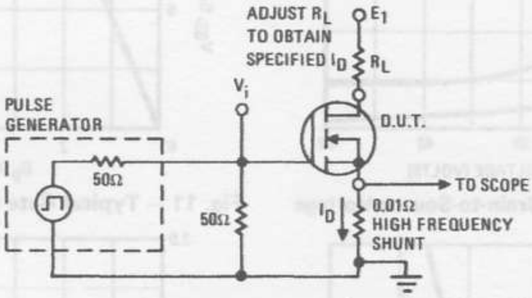


Fig. 17 – Switching Time Test Circuit

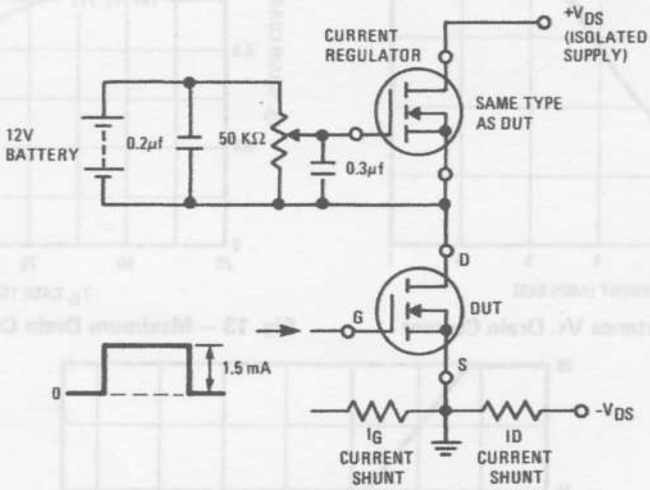


Fig. 18 – Gate Charge Test Circuit