HUGHES MICROELECTRONICS LIMITED

CMOS Digital Frequency Synthesizer

HCTR 0320/0320A

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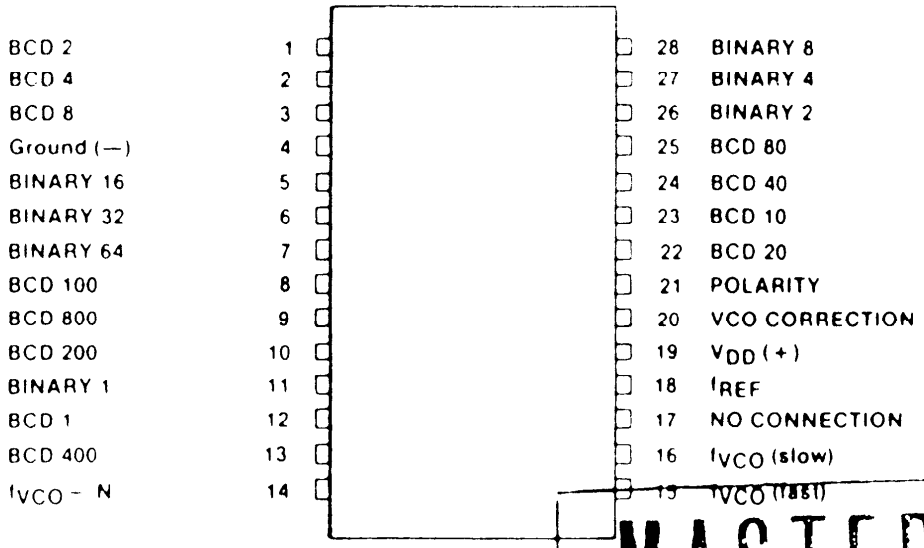
DESCRIPTION

The HCTR0320 is a CMOS LSI programmable divide by N counter with a phase/frequency detector for frequency synthesis or phase locked loop (PPL) applications. A minimum PLL system can be made using the HCTR0320, a reference oscillator and divider, low pass filter, and voltage controlled oscillator (VCO). More complex systems may use mixers, frequency multipliers, or a dual modulus prescalar. Most system designs constrain the VCO to oscillate at N times the divided reference oscillator frequency (f_{REF}) so changing N by ΔN changes the VCO frequency by the product $(\Delta N) \cdot (f_{REF})$. Thus multi- VCO frequencies can be generated from only one reference oscillator crystal by varying N. This method results in VCO frequencies which have the same fractional error as the reference crystal oscillator frequency.

FEATURES

- HIGH FREQUENCY OPERATION (8MHZ)
- LOW POWER CMOS
- ON CHIP PHASE/FREQUENCY DETECTOR
- BCD AND/OR BINARY INPUTS FOR N
- ON CHIP ADDER TO PROVIDE OFFSET
- N PROGRAMMABLE FROM 3 TO 1023
- VCO SIGNAL PRECONDITIONING
- OUTPUT FROM – N COUNTER IS PROVIDED
- POLARITY CONTROL ON VCO CORRECTION SIGNAL



ABSOLUTE MAXIMUM RATINGS	SYM.	VALUE	UNIT
DC Supply Voltage	V_{DD}	+ 15 to –0.3	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to –0.5	Vdc
DC Current Drain Per Pin, All Inputs*	I	10	mAdc
DC Current Drain Per Pin, All Outputs*	I	20	mAdc
Operating Temperature Range	T_A	–40 to 85°C	oC
Storage Temperature Range	T_{stg}	–65 to + 150	oC
Power Dissipation	Pd	600 (plastic pkg) 700 (ceramic pkg)	mW

* Protection diodes forward biased

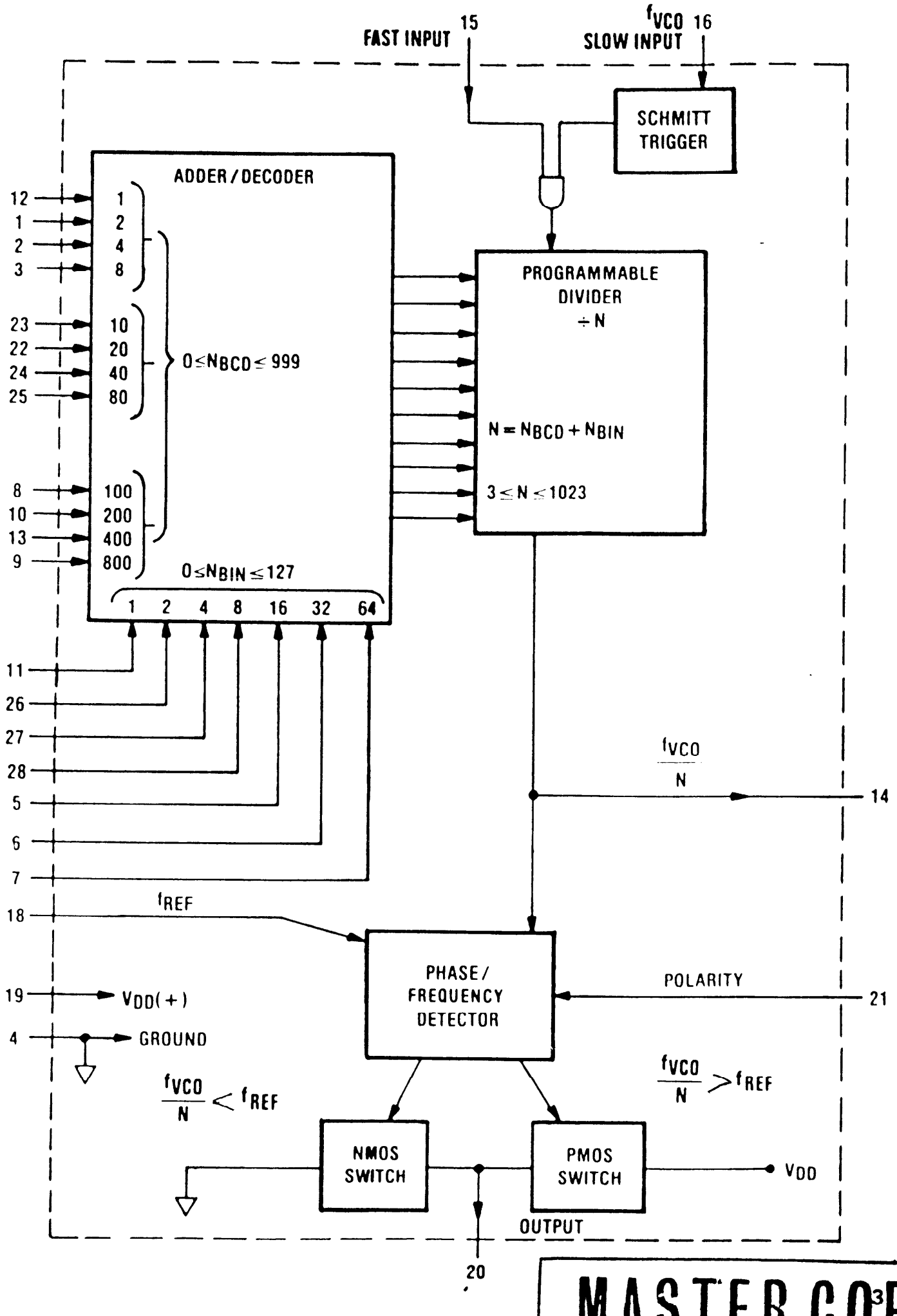
EXPLANATION OF BLOCK DIAGRAM

Adder/Decoder - This block adds a three digit BCD number (N_{BCD}) to a 7 bit binary number (N_{BIN}) to provide a sum equal to the division integer (N). Each decade of BCD inputs is restricted to valid BCD numbers, zero through nine. The Binary and BCD inputs require full swing signals such as those achieved by SPDT switches or CMOS logic. Positive logic is used.

Programmable Divider - This circuit utilizes a continuously recycling presettable down counter to output a waveform of frequency $f_{VCO/N}$ at a duty cycle of 1/N. f_{VCO} (fast) is the only TTL compatible input and should be used when fast rise and fall times are available and/or maximum speed is required. For input signals with slow rise and fall times such as sine waves, the f_{VCO} (slow) input provides signal preconditioning through a Schmitt Trigger in order to obtain proper rising and falling edges for the digital circuitry. However, the additional circuitry does restrict the maximum operating frequency. The unused f_{VCO} input must be connected to V_{DD} (+). Either f_{VCO} input will accept low frequencies. However, in order to obtain high operating frequencies, dynamic circuitry is used and thus the minimum guaranteed f_{VCO} input frequency is 5 KHz.

Phase/Frequency Detector - This block compares the divider output ($f_{VCO/N}$) with an external reference frequency (f_{REF}) and generates a correction signal. When the VCO correction output goes from the floating state (NMOS and PMOS switches-off) to V_{DD} (+) or GND (—), the indication is that the leading edges of the two input signals do not occur simultaneously. The leading edge of one signal triggers the correction pulse and the leading edge of the other signal resets the output to the floating state (Refer to Timing Diagram). Therefore, the width of the correction pulse is proportional to the time difference between the leading edges. As the two signals approach equal frequency and phase, the width of the pulse becomes narrower and narrower and the two signals are in "lock". The Polarity input should be tied to V_{DD}(+) if the VCO correction output voltage should decrease to cause an increase in the VCO frequency.

CMOS DIGITAL FREQUENCY SYNTHESIZER BLOCK DIAGRAM



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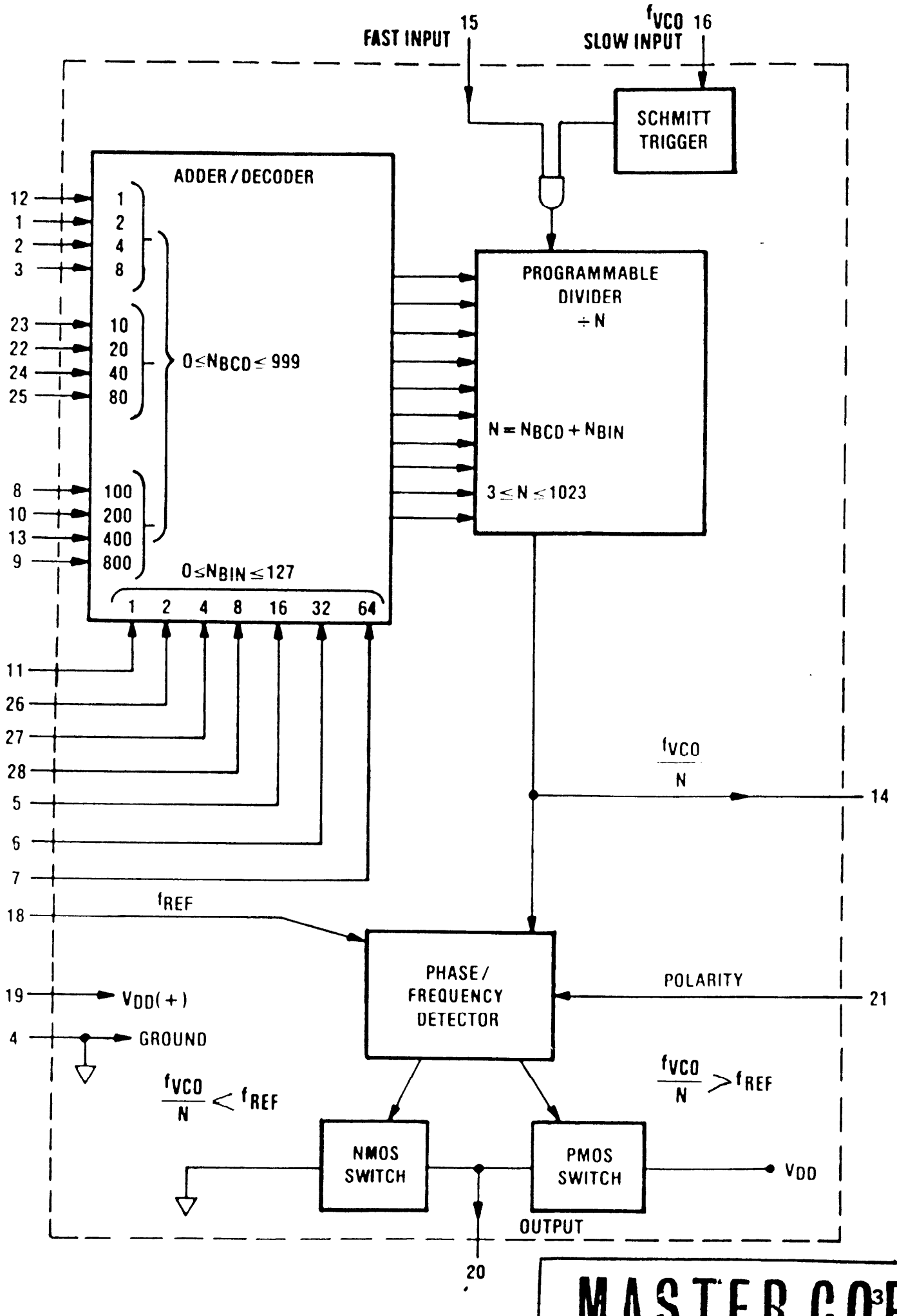
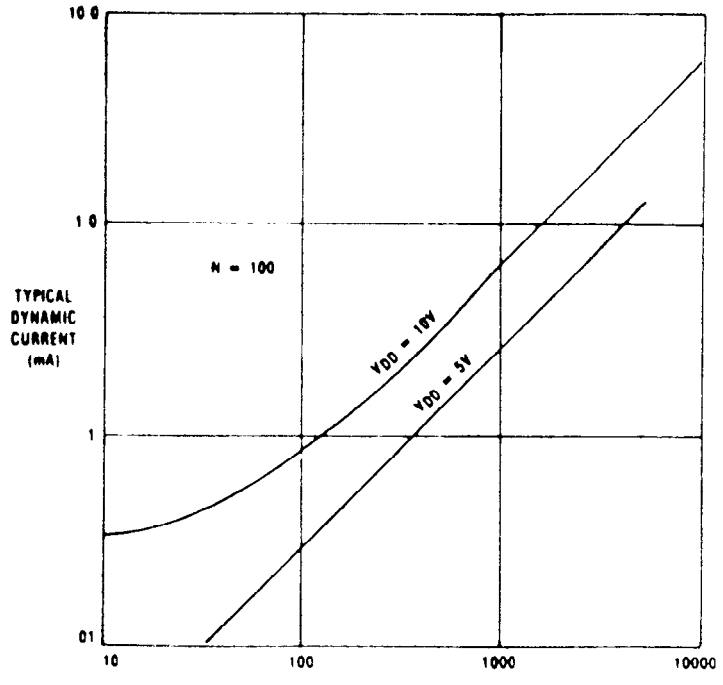
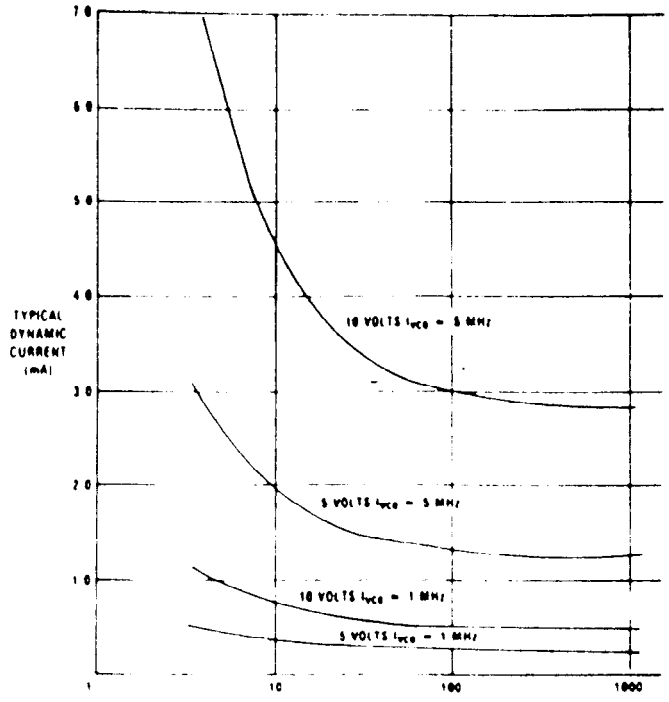


ELECTRICAL SPECIFICATIONS · Unless otherwise specified T = −40°C to 85°C V_{DD} tolerance = ± 5%

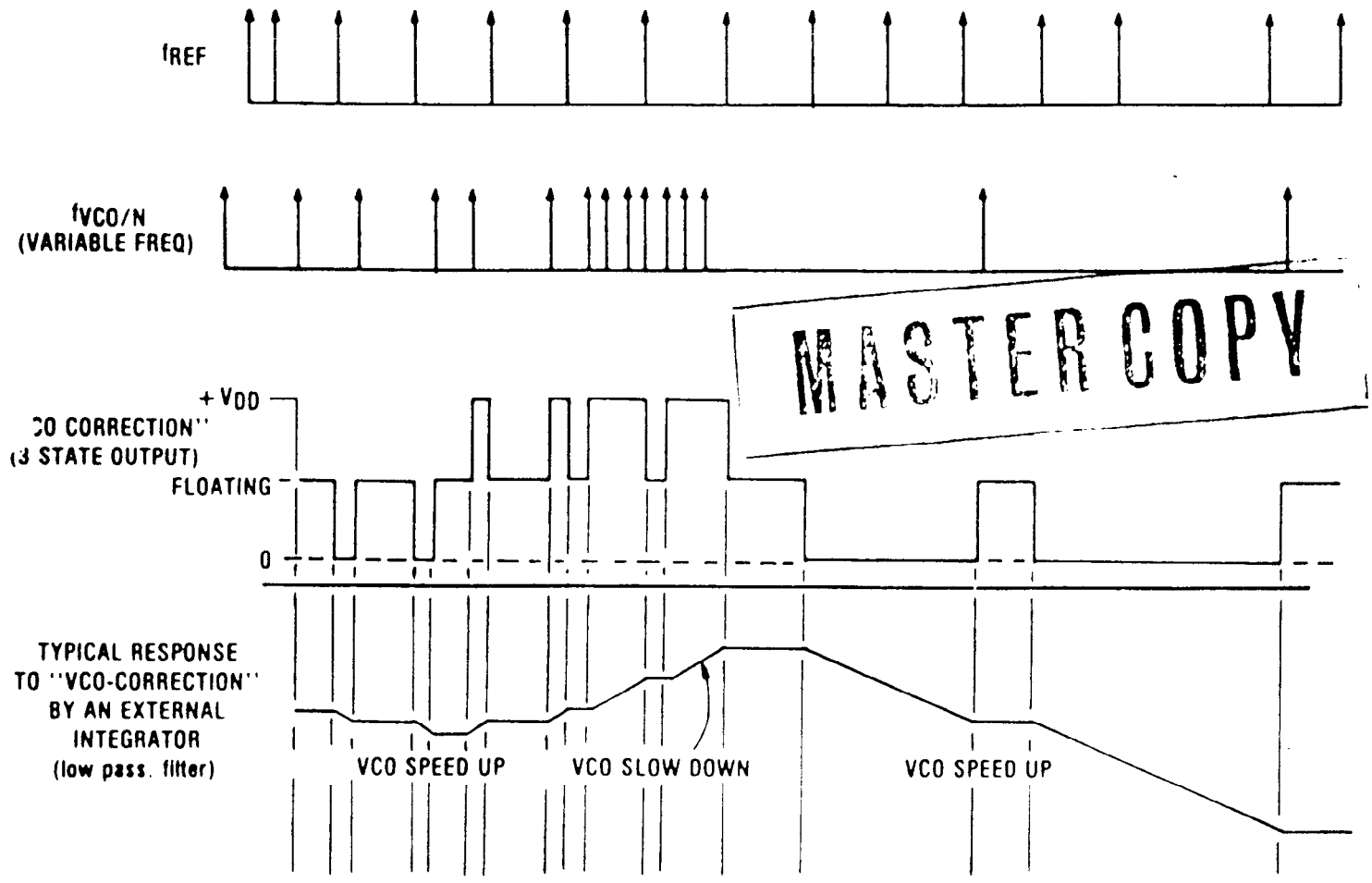
D C CHARACTERISTICS		SYMBOL	CONDITIONS	V_{DD}	MIN	MAX	UNITS
Supply Voltage		V_{DD}	HCTR 0320		4.5	13	V
Input Levels			HCTR 0320A		4.5	10	V
BCD and Binary Switches	"1"	V_{IH}		5	4.75	5	V
				10	9.75	10	V
	"0"	V_{IL}		5	0	.25	V
(50 KΩ Impedance required)				10	0	.25	V
f_{VCO} (Fast)	"1"	V_{IH}		5	3.5	5	V
				10	7	10	V
	"0"	V_{IL}		5	0	.4	V
				10	0	1.0	V
f_{VCO} (Slow), f_{REF}	"1"	V_{IH}		5	4.5	5	V
				10	9	10	V
	"0"	V_{IL}		5	0	.5	V
				10	0	1.0	V
Input Leakage Current		I_L	To either V_{DD} or GND	5	—	1	μA
(except BCD and Binary inputs)				10	—	2	μA
Input Capacitance		C_I	(Typical)			5	pf
Output Impedance, f_{VCO}/N and VCO Correction		R_{on}	Within 1 Volt of supply	5	—	500	Ω
				10	—	360	Ω
		R_{off}			5	—	MΩ
A C CHARACTERISTICS (NOT 100% PRODUCTION TESTED)							
Supply Current		I_{DD}	f_{VCO} = 1 MHz	5	—	.5	mA
			N = 100	10	—	1.0	mA
Inputs							
f_{VCO} (Fast) frequency		F_{VCO}		5	005	3.5M	MHz
				10	010	8	MHz
pulse width		PW_H	50% to 50%	5	120	100	μs
		PW_L		10	055	50	μs
rise & fall time		t_r, t_f	10% to 90%	5	—	100	ns
				10	—	50	ns
f_{VCO} (Slow) frequency		f_{VCO}		5	005	2.5	MHz
				10	010	5	MHz
pulse width		PW_H	50% to 50%	5	200	100	μs
		PW_L		10	100	50	μs
rise & fall time		t_r, t_f	10% to 90%	5	No limit		
				10			
f_{REF} pulse width		PW_H	50% to 50%	5	300	—	ns
		PW_L		10	150	—	ns
rise & fall time		t_r, t_f	10% to 90%	5	-	1	μs
				10	-	1	μs
Outputs							
f_{VCO} (Slow) to f_{VCO}/N propagation delay, falling edge to rising edge		t_{pH}	50% to 50%	5	—	750	ns
			C_L = 10 pf	10	—	420	ns
falling edge to falling edge		t_{pL}	50% to 50%	5	-	680	ns
			C_L = 10 pf	10	-	375	ns
f_{VCO} (fast) to F_{VCO}/N propagation delay, falling edge to rising edge		t_{pH}	50% to 50%	5	—	360	ns
			C_L = 50 pf	10	—	250	ns
falling edge to falling edge		t_{pL}	50% to 50%	5	—	315	ns
			C_L = 50 pf	10	—	270	ns



FREQUENCY — f_{VCO} (KHz)



+ N



NOTES: 1. ONLY POSITIVE TRANSITIONS OF f_{REF} AND f_{VCO} ARE SHOWN. CIRCUIT OPERATION IS INDEPENDENT OF DUTY CYCLES.
2. POLARITY SENSE IS TIED TO V_{DD}

TIMING DIAGRAM OF PHASE FREQUENCY DETECTOR